Performance Characterization of FPGA Techniques for Calibration and Beamforming in Smart Antenna Applications

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***Abstract*—A field-programmable gate array (FPGA) implementation is presented for a smart antenna application employing digital beamforming. The digital beamforming is performed at the RF signal carrier frequency by means of bandpass (IF) sampling, using high-speed 8-b analog-to-digital converters. The digital phased array receiver presented in this paper consists of an eight-channel system with back-end FPGAs for calibration and digital beamforming processing. The system operates in the *L*-band (1.8–2 GHz) with various bandwidths depending on the application and FPGA processing requirements. This paper focuses on two main topics, calibration methodologies and FPGA implementation for calibration and digital beamforming, and includes several performance trades. Results presented include real measured data that were collected with the system and processed via FPGAs.**

***Index Terms*—Adaptive arrays, array signal processing, calibration, field-programmable gate arrays (FPGAs).**

I. Introduction

EXPERIENCE gained in the area of digital phased array processing suggests that the optimal smart antenna receiver requires a front-end antenna array followed by an analog-to-digital converter (ADC) behind every element. All channels would then be processed using some type of real-time engine. Flexibility, complexity, and form factor dictate that a combination of IF sampling techniques (to minimize the amount of RF electronics) and field-programmable gate array (FPGA) technology (for size and flexibility) be used to comprise an array-based antenna receiver architecture. Such an architecture would be capable of serving a wide variety of applications from direction finding in wide-band radar processing to co-channel interference mitigation in narrow-band personal communications systems (PCS).

While smart antenna (array) processing concepts have been around for some time [1], only recently has the technology become available, making the above notion of an optimal smart antenna receiver hardware implementation a real possibility. Indeed, recent efforts indicate a growing interest by researchers in such an optimal implementation. In [2] and [3], the authors introduce efficient algorithms for smart antenna processing to facilitate FPGA implementation. Along the same lines in [4] and [5], the authors trade co-channel interference mitigation performance against smart antenna algorithm approaches when implemented separately in FPGA systems.

In addition to this work, which generally addresses implementation at the system level, some authors have studied some of the lower level issues impacting practical implementation such as mutual coupling and calibration [6]–[12]. There are a number of such issues like this that must be addressed before the optimal smart antenna receiver can be practically realized. Some of these include digital logic implementation approaches (driving speed, complexity, and precision), analog-to-digital (A/D) conversion (including speed, number of bits, and optimal loading), and IF sampling techniques and supporting electronics (frequency plan). The work discussed in this paper extends the state of development in this area by taking a comprehensive approach to addressing these four areas that comprise the key performance drivers for practical implementations of optimal smart antenna receivers. Specifically, this paper will present the results of one such smart antenna hardware implementation, the design of which has been optimized based on the above performance drivers.

The system under study is an eight-channel system implemented in hardware with near real-time FPGA processing capability [13], [14]. The paper is organized as follows. First, an overview of the system will be presented describing the hardware elements of the smart antenna. Following the system overview, calibration methodologies that were used to calibrate the smart antenna will be discussed. The last section of the paper will focus on the FPGA implementation including calibration and digital beamforming. Measured results are presented for both calibration techniques and FPGA processed data.

II. Smart Antenna Receiver System Overview

A block diagram of the eight-channel digital smart antenna receiver system is shown in Fig. 1. Maximum operational system bandwidth is 200 MHz, from 1.8 to 2.0 GHz, but due to FPGA limitations the actual real-time processed bandwidth will be lower. Bandwidth limitations due to the FPGAs are discussed in Section IV along with the FPGA implementation. The system analog front-end consists of an eight-element linear half-wave dipole array where each element is followed by a low-noise amplifier (LNA), automatic gain control (AGC), and bandpass filter (BPF). After each analog channel, the RF signal is digitized using a high-speed 8-b ADC with a maximum

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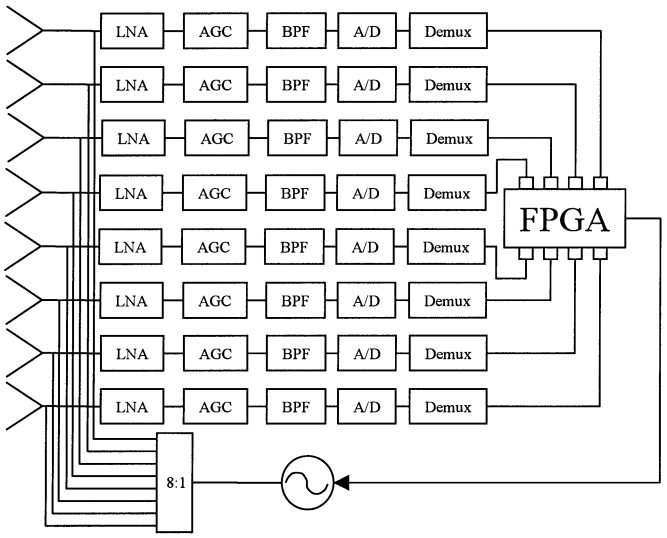

Fig. 1. Smart antenna system with calibration including only the hardware chain.

sampling rate of 1.5 Gs/s and 2.2-GHz RF bandwidth. For some of the results presented in this paper, the maximum sampling rate was set to 1 Gs/s and data was captured on a logic analyzer. For these high sampling rates, before the data can be passed to the FPGA the data must first be demultiplexed to a slower clock speed compatible with the FPGA. As an example, for full system capability with 200-MHz bandwidth, the best sampling frequency with the most guard band would be 845 MHz [15]. This produces a sampled IF center frequency of 210 MHz. With an 845-MHz sampling clock rate, a demux of $1:8$ would be necessary to slow the data to 105.625 MHz, allowing it to be implemented in a Xilinx Virtex-II FPGA [16]. In the hardware implementation, the operational bandwidth is limited to 25 MHz with an A/D clock speed of 80.842 MHz, allowing for 7.5 MHz of guard band on both sides of the spectrum. The clock speed is compatible with the Xilinx Virtex-E FPGA [17] used in this system and relaxes the need for any demultiplexing between the ADC and the FPGA.

Next, we present the algorithm for implementing digital beamforming, including calibration, in the smart antenna receiver system. Starting with the received RF signals, $s_{m,n}$, collected from the antenna array and passed through the RF chain, we first quantize each channel with an 8-b ADC

$$q_{m,n} = \text{quantize}(s_{m,n}) \tag{1}$$

where

$$m = 1, 2, \ldots, M \quad \text{and} \quad n = 1, 2, \ldots, N. \tag{2}$$

M is the total number of channels or ADCs, and N is the total number of sample points or fast Fourier transform (FFT) points. For the system presented here, $M = 8$ and $N = 16$, 64, 256, or 1024. The quantization is performed via bandpass (IF) sampling where the proper sampling rates are computed from [15]

$$f_S = \frac{(f_{\mathrm{U}} + B_{\mathrm{GU}})}{n} + \frac{(f_{\mathrm{L}} - B_{\mathrm{GL}})}{n-1} \tag{3}$$

where

$$n = \text{floor}\left(\frac{f_{\mathrm{U}} + B_{\mathrm{GU}}}{f_{\mathrm{U}} - f_{\mathrm{L}} + B_{\mathrm{GU}} + B_{\mathrm{GL}}}\right). \tag{4}$$

f_{L} and f_{U} are the lower and upper RF frequency limits and B_{GL} and B_{GU} are the lower and upper guard bands, respectively. For example, this FPGA implementation has $f_{\mathrm{L}} = 1907.5$ MHz, $f_{\mathrm{U}} = 1932.5$ MHz, and $B_{\mathrm{GL}} = B_{\mathrm{GU}} = 7.5$ MHz, resulting in $f_S = 80.842$ MHz.

After quantizing (1), an FFT is performed on each channel to transform the data from time-domain sampled space to the frequency-domain sampled space

$$Q_{m,n} = \text{FFT}(q_{m,n}). \tag{5}$$

At this point, the data are calibrated to align all channels in amplitude and phase. This is easily accomplished in the frequency domain by simply applying an amplitude and phase weight as follows:

$$Q_{m,n}^{\mathrm{CAL}} = Q_{m,n} a_m e^{-j\phi_m} \tag{6}$$

where the phase correction weights are given as

$$\phi_m = 2\pi f_0 \tau_m \tag{7}$$

measured at the RF center frequency f_0. Since the fractional bandwidth of the RF channel is small, the phase variation across the channel is minimal. a_m and τ_m are the amplitude and time delay weights for each channel. To simplify hardware implementation, ϕ_m is held constant across the frequency, which causes small errors in phase near the band edges.

The final step is the actual digital beamforming, which is accomplished by the matrix multiplication

$$T_{k,n} = A_{k,m} Q_{m,n}^{\mathrm{CAL}} \tag{8}$$

where $A_{k,m}$ is a matrix containing amplitude and phase weights for the antenna beam shape and scanning, given as

$$A_{k,m} = b_m e^{-j2\pi(m-1)(d/\lambda_0)\sin(\theta_{s_k})}. \tag{9}$$

The total number of simultaneous antenna beams is K, where $k = 1, 2, \ldots, K$ with θ_{s_k} representing the scan direction of each beam. The other elements given in (9) include the amplitude taper weights b_m, the antenna spacing d, and the free space wavelength λ_0. The system presented here uses $K = 25$, $b_m = 1$, and $d = 3$ inches for center frequency operation at 1.92 GHz. In Section IV, we will explain how this digital beamforming algorithm, including the application of calibration channel weights, is implemented in the FPGA.

III. Calibration Techniques

One of the main advantages of having a smart antenna with digital control over every element in the array is the ease with which calibration can be implemented. In a practical system, it is difficult to balance the amplitude and phase of every channel over temperature and frequency. Accurate alignment of channels would require high-precision hardware components which would accrue system cost. For comparison, a digital smart antenna has the ability to balance the channels using digital pro-

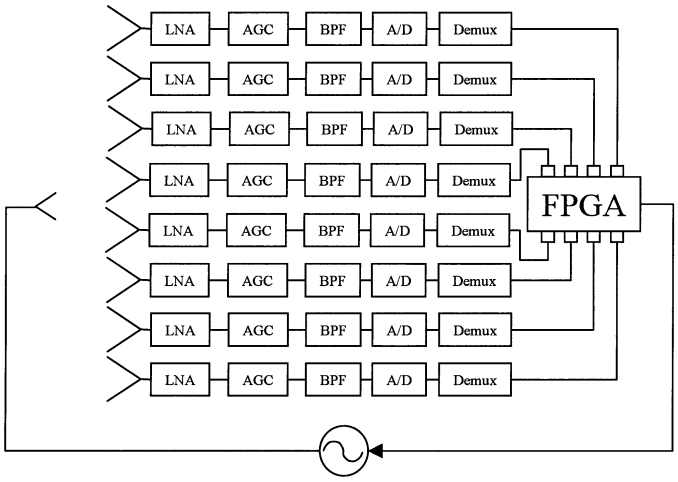

Fig. 2. Smart antenna system with calibration including the antenna array and hardware chain.

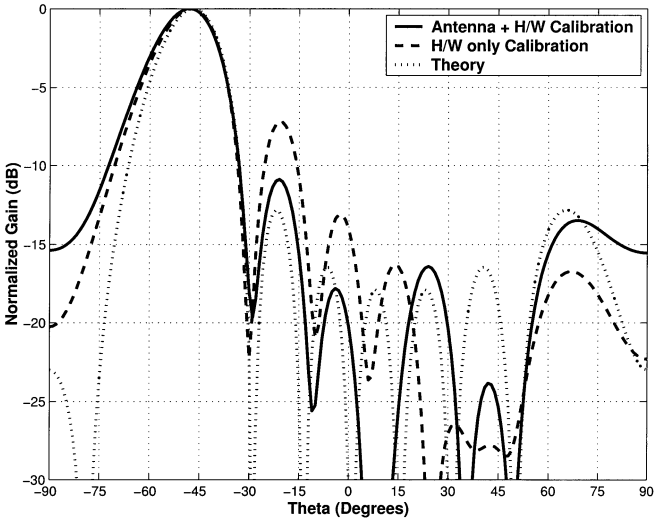

Fig. 3. Antenna pattern cut at -47° scan for both calibration methods shown in Figs. 1 and 2.

cessing techniques, allowing for cheaper hardware components to be used. For the digital smart antenna system presented here, two calibration methods will be compared.

The first calibration method is shown in Fig. 1. A calibration signal is generated and split eight ways and passed through each channel. These eight signals are injected into each channel through a switch which is not shown in Fig. 1. Each signal is then passed through the RF hardware, digitized, and fed to the FPGA. In the FPGA, the amplitude and phase shifts associated with each channel are computed. Given a reference channel, the appropriate phase shifts and normalized amplitudes between all channels are computed. Once these values are known, they are applied to each respective channel during the digital beamforming processing. This calibration procedure can be applied anytime the system is not collecting data. Due to temperature changes, the smart antenna system may need to calibrate several times throughout the day. The calibration signal used here was a continuous wave (CW) tone, but is not limited to such a signal and more sophisticated signals could be used [7], [12].

The previous calibration method is well proven and works, but neglects the effects of the radiating antenna elements. The mutual coupling of the antenna elements could be added [18]–[20], but they would need to be known by either measurement or simulation. One other concern with the above calibration method is the degradation in noise figure due to the switch in front of the LNA. To avoid both of these issues, the smart antenna system could be calibrated using the method shown in Fig. 2. Here, instead of taking the calibration signal and splitting it into each channel, a small antenna probe is placed in front of the antenna in the far field at broadside. With this technique, the mutual coupling effects due to the antenna are included in the calibrated signal. The biggest concern with this method is accurately aligning the calibration antenna probe in front of the smart antenna system and also having it in the far field. Any calibration signal type could be used for this method as well.

An experiment was performed to compare both calibration techniques, and the results are shown in Fig. 3. Note that, for these experiments, the data was processed off-line and not with the FPGAs. The calibration signal was a 1.92-GHz CW tone and the sampling rate of the ADC was 1 Gs/s. With this calibration signal, the smart antenna was calibrated using both methods. For the first experiment, a signal centered at 1.92 GHz was transmitted to the smart antenna system with an angle of arrival equal to -47°. This signal was captured and processed off-line using the calibration weights computed from each method. Fig. 3 shows the processed measured results, where it can be seen that the calibration method shown in Fig. 2 compares more favorably with theory than the calibration method shown in Fig. 1.

IV. FPGA Implementation

The next two subsections will present the FPGA implementation of the smart antenna system for performing calibration and digital beamforming for all eight channels. The FPGA platform (Wildstar VME, Annapolis Microsystems) used consists of five Xilinx Virtex-E (XCV1000E) [17] FPGAs, where each FPGA has 1.5 million gates, 12 288 slices, and 393 216 b of block RAM. The FPGAs were programmed using a combination of Xilinx cores and custom very high-speed integrated-circuit (VSIC) hardware design language (HDL) (VHDL) code. The limitations in implementing digital beamforming processing on the FPGA platform include the I/Os between the individual FPGA chips and after the output, and the device size and speed needed to implement the algorithms. Due to these limitations, it was necessary to perform sections of the digital beamforming operation serially and therefore required that the system be operated in near real time mode (one eight-channel snapshot of 12.7 μs collected approximately every 495 μs).

A. Calibration

The FPGA calibration procedure for a single channel is shown in Fig. 4. Given 8-b time-domain data samples from the ADC, the FFT performs a Cooley–Tukey radix-4 decimation-in-frequency FFT (comprised of five ranks of 256 butterfly operations) and outputs 16-b frequency domain data samples

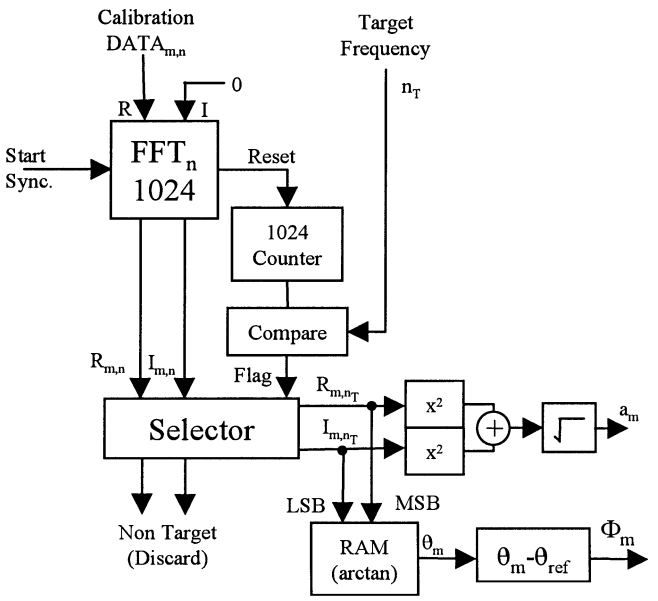

Fig. 4. FPGA procedure for computing calibration weights, amplitude, and phase, for each channel of the smart antenna system.

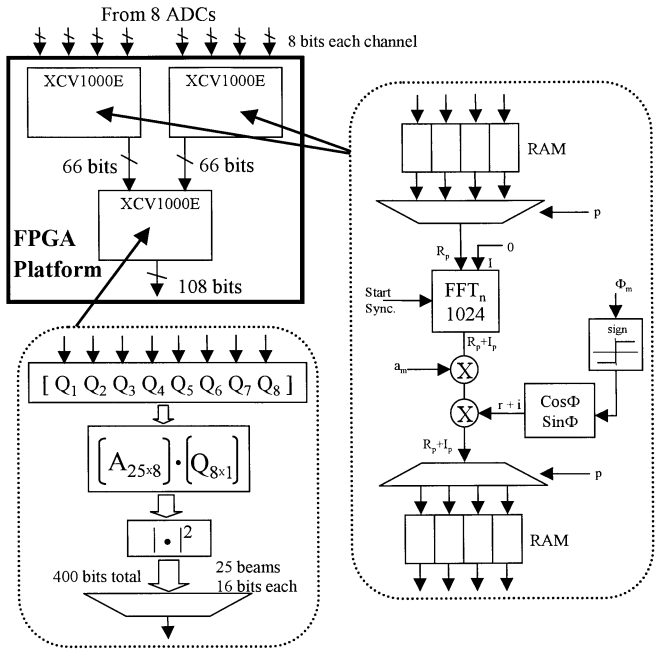

Fig. 5. FPGA architecture for applying channel calibration weights and computing digital beamforming matrix.

for both the real and imaginary components (imaginary inputs are tied to zero). These outputs are fed into a selector that picks out the complex pair corresponding to a target frequency (occupied by the calibration tone). The magnitude and phase a_m and ϕ_m of this pair are then computed and stored as a calibration amplitude-phase pair. Note that ϕ_m is computed from the phase of the individual channel θ_m with respect to the reference channel $\theta_{\rm ref}$. The square root operation is implemented using the coordinate rotation digital computer (CORDIC) algorithm. The $\arctan$ is found using a table in RAM. There are many ways this calibration calculation scheme could be further automated. It would be a straightforward process to merely search for the frequency containing the most signal energy and perform the calibration there. This would allow a swept frequency signal to be delivered to the front end of each channel and provide for rapid wide-band calibration data.

B. Digital Beamforming

The digital beamforming FPGA processing is done in two parts. First, the calibration weights are applied using (6), and second, the eight channels are beamformed through a matrix multiplication given by (8).

The calibration correction implementation is shown in Fig. 5. Given a current calibration set (comprised of eight amplitude weights and eight phase shifts), it is a straightforward though nontrivial process to apply the calibration to data arriving from the ADCs. Each calibration block is designed to take inputs from four ADCs (for eight array elements, two calibration blocks are needed). Each calibration block consists of four RAM blocks which allow for four channels of simultaneous data to be captured in near real time. Each calibration block consists of a 1024-point FFT (shared between the four RAM blocks using a multiplexer), and a $\sin/\cos$ lookup table. After the 8-b ADC data is captured in RAM, each channel is individually processed through the FFT and 16-b frequency-domain data is generated. These outputs (real and imaginary) are each multiplied by the a_m for the current channel, thus correcting for any deviations in magnitude. Concurrently, ϕ_m (constant phase shift per channel stored as a 10-b number) is sent to a $\sin/\cos$ lookup table with the appropriate sign to account for positive and negative frequencies. The lookup table outputs 12-b values which alter the real and imaginary amplitude corrected signals by performing a complex multiplication (requires four real multiplies and two additions). Output samples are now compensated for unwanted amplitude and phase variations using the weights computed during the calibration process. Each channel (four per block) goes through the calibration process serially and is stored in RAM as complex data until all channels are processed. All of this processing (four channels) is located on a single FPGA using 25% of the slices, 33% of the block RAM.

The calibration for eight antenna elements is performed on two FPGAs and subsequently passed to a third FPGA for the beamforming operation. The data is passed between the FPGAs in parallel mode because of the requirement to have all channel data present simultaneously for the beamforming operation. The FPGA system on which the design was implemented (see Fig. 5) limits the number of bits output from the FPGAs to 66 b, therefore, for four channels, only 8-b real and 8-b imaginary data can be passed from each FPGA. This requires significant truncation before the data is passed onto the beamforming operation. A custom FPGA board could easily alleviate this limitation.

The beamforming operation requires a large complex matrix multiplication given by

$$[\mathbf{T}]_{\mathbf{25\times1024}} = [\mathbf{A}]_{\mathbf{25\times8}}[\mathbf{Q^{CAL}}]_{\mathbf{8\times1024}} \tag{10}$$

where $\mathbf{Q^{CAL}}$ represents the calibrated FFT data of all eight channels, $\mathbf{A}$ represents the beam scanning matrix weights given by (9), and $\mathbf{T}$ represents the beamformed data output. Note that

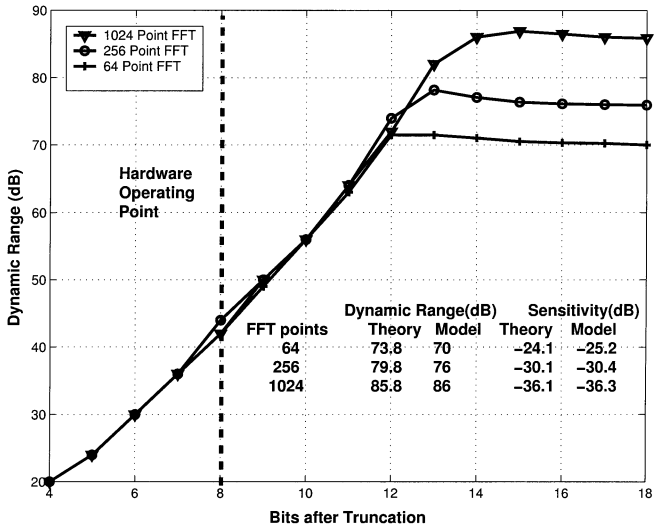

Fig. 6. FPGA system dynamic range due to bit truncation caused by system I/O limitations. The inset table shows the theoretical dynamic range and sensitivity limits compared to those for the MATLAB FPGA model (using no truncation) versus FFT size.

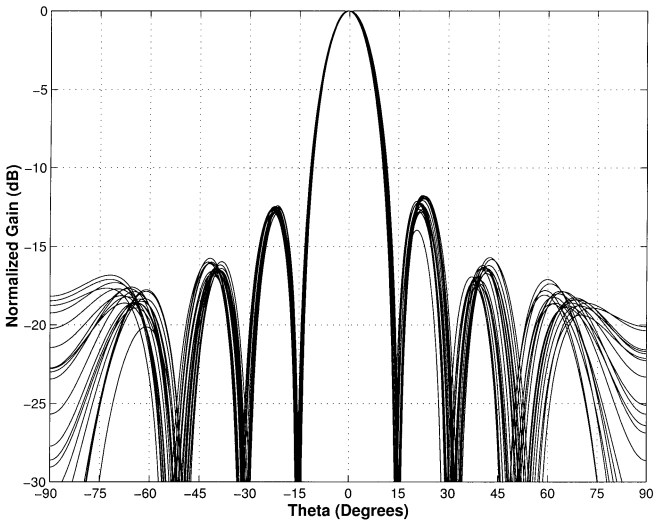

Fig. 7. Broadside calibrated antenna patterns over the full system bandwidth (1.8–2 GHz).

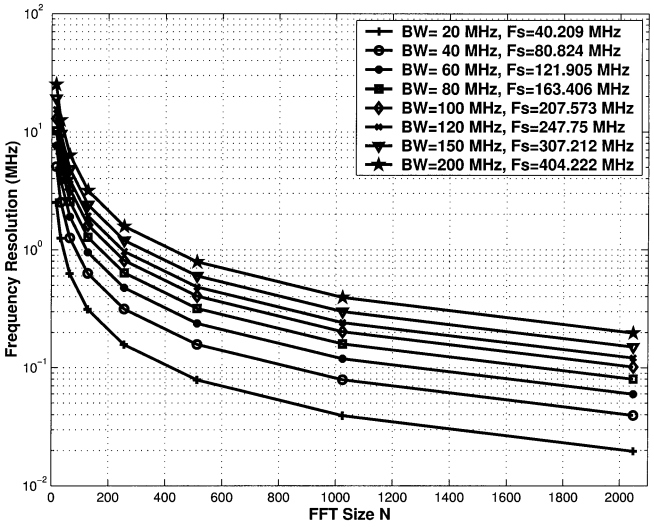

Fig. 8. Calculated FFT frequency resolution for several sampling rates with maximum bandwidths.

there are a total of 1024 samples per data stream, 25 scan angles ($-60°$ to $+60°$ in $5°$ steps), and eight channels.

Eight new complex samples are received every clock period from the data streaming out of the channel correction blocks. These eight complex numbers comprise one column of the $\mathbf{Q^{CAL}}$ matrix. The clock period when they arrive at the beamforming block indexes the columns of the $\mathbf{Q^{CAL}}$ matrix (frequency). Thus, each clock period needs only to calculate the results for one column of the $\mathbf{T}$ matrix by using only one column from the $\mathbf{Q^{CAL}}$ matrix. Unfortunately, this calculation requires each value in the $\mathbf{A}$ matrix and therefore the entire matrix must be stored within the FPGA. The $\mathbf{Q^{CAL}}$ matrix data and $\mathbf{A}$ matrix data are both complex and thus complex multiplies and twice the storage are required. For direction finding, only the magnitude of the power spectrum is necessary and therefore the real and imaginary parts of the output are squared and summed. The magnitude data is truncated to 16 b producing 400 outputs bits (for all 25 angles) every clock cycle. The FPGA I/O is limited to 108 b (see Fig. 5), therefore taking four clock cycles to remove all of the data due to one column of the $\mathbf{Q^{CAL}}$ matrix. The matrix multiplication is resource intensive and therefore a primary driver for determining the number of scan angles used. Several trades were made to determine the $\mathbf{A}$ matrix size and number of $\mathbf{A}$ matrix bits. As an example, 6 b and 25 angles use 10 691 FPGA slices (87% of chip), 6 b and 13 angles use 7199 slices (59% of chip), and 10 b and three angles use 2914 slices (24% of chip).

C. Dynamic Range

Dynamic range and signal sensitivity are important parameters in digital beamforming applications. For direction finding, it is desirable to not only be able to detect the signals, but do so over a wide range of power levels. The dynamic range performance of the digital beamforming system depends on whether the input signals have spatial or spectral separation. The dynamic range for spatial separation (different arrival angle but same frequency) is limited to roughly 13 dB (assuming no amplitude tapers) due to the sidelobes of the antenna pattern. However, for different frequencies, the fundamental limit of the dynamic range is set by the digitizer and digital array processing. The number of ADC bits, the number of points in the FFT, and the number of array elements each contribute to the dynamic range. The ADC introduces a noise floor into the system due to quantization errors. The FFT effectively filters the noise into individual bins and the elements of the array combine the signals coherently (noise incoherently) giving the following equation for theoretical dynamic range performance

$$DR\ (\text{dB}) = 6b + 1.75 + 10\log_{10}\left(\frac{N}{2}\right) + 10\log_{10}(M) \quad (11)$$

where b is the number of bits, N is the size of the FFT, and M is the total number of channels. The theoretical sensitivity performance of the system is also determined by the digital array

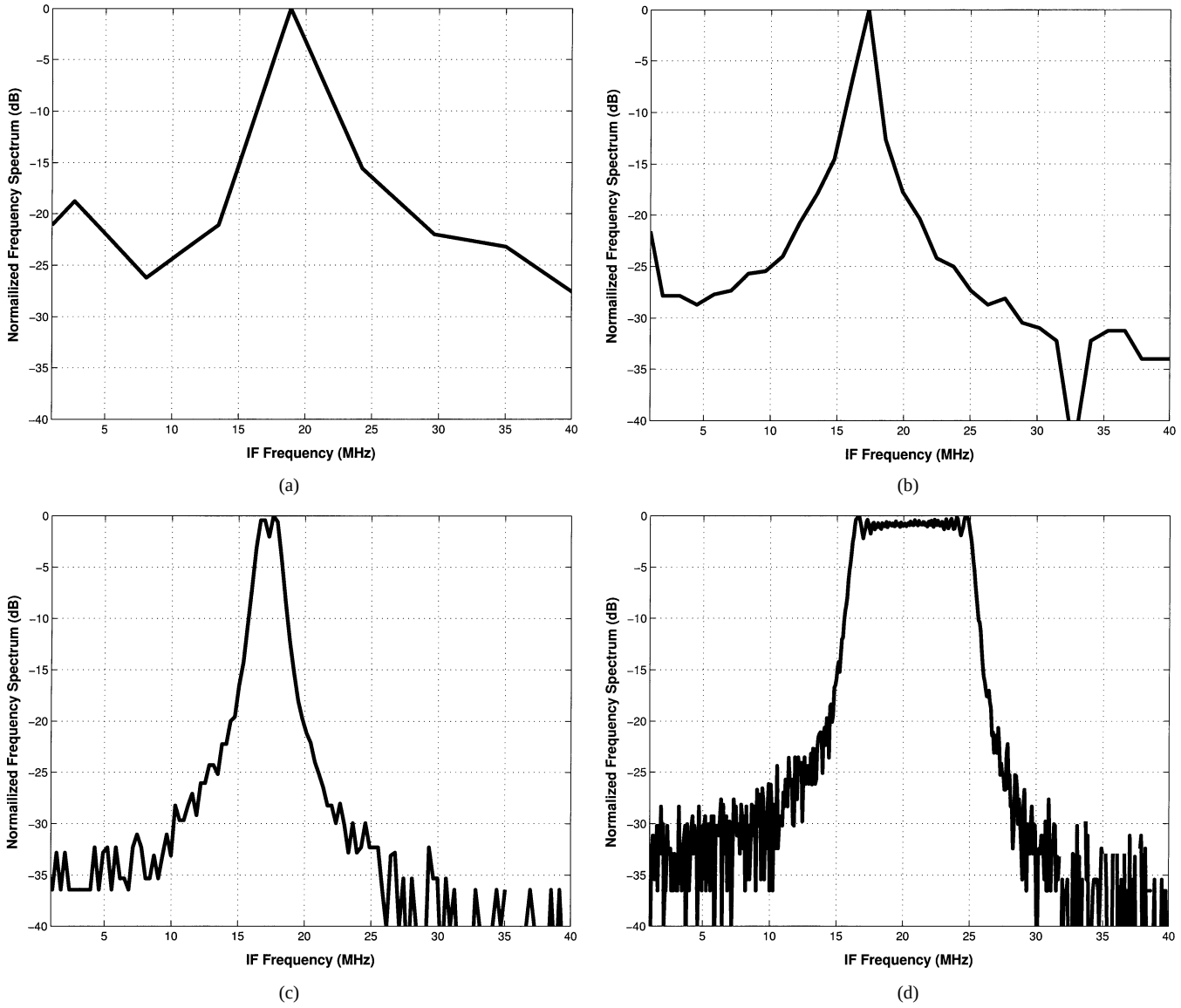

Fig. 9. Frequency spectrum for a single-channel 10-MHz linear FM waveform. (a) 16-point FFT. (b) 64-point FFT. (c) 256-point FFT. (d) 1024-point FFT.

processing as described above, and the required SNR at the A/D input to detect a signal is given by

$$SNR_{ADC}\ (\text{dB}) = -10\log_{10}\left(\frac{N}{2}\right) - 10\log_{10}(M) \qquad (12)$$

where N and M are the same as above.

Both of these equations are based on the threshold for detection being the mean noise power outside the signal of interest (i.e., signal power $=$ noise power). These two equations show that dynamic range and sensitivity can be increased by increasing any one of the A/D bits, FFT points, or array elements. The number of A/D bits and number of array elements are determined by hardware and thus difficult to modify (essentially fixed) once a system is integrated. However, the FFT is part of the FPGA processing and its size can more easily be varied by changing the digital processing algorithms. From (11) and (12) and Fig. 6, it is clear that using the largest FFT will improve dynamic range and sensitivity. It is important to note that the dynamic range and sensitivity performance changes if the signal

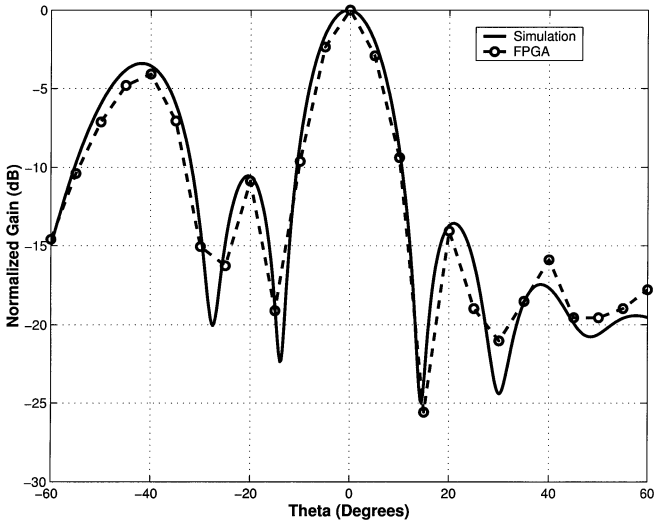

Fig. 10. Processed antenna pattern cut for a two-tone input comparing the FPGA data to simulated data.

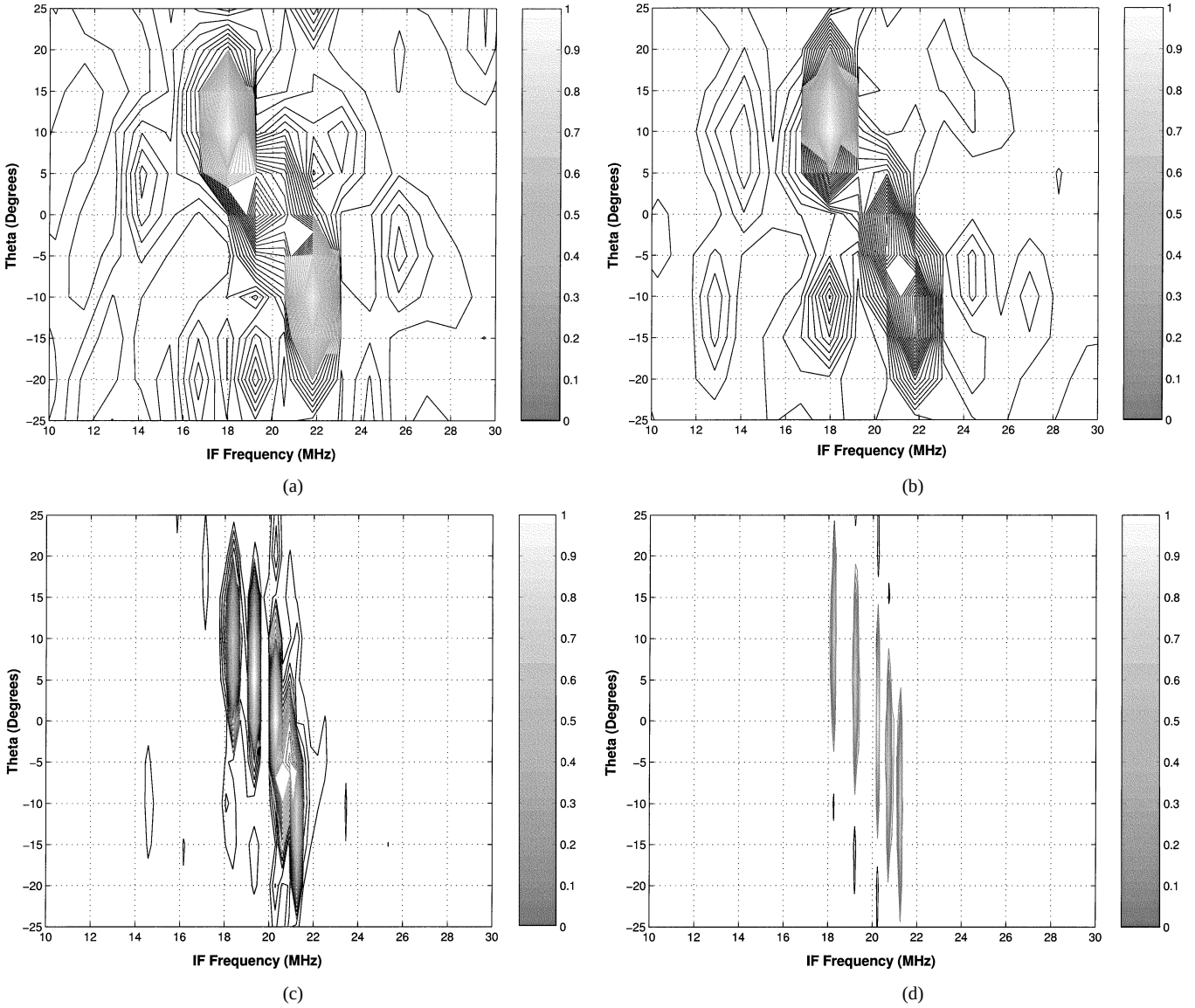

Fig. 11. Digital beamformed contour plots for five received signals at different angles of arrival and frequencies. (a) 16-point FFT. (b) 64-point FFT. (c) 256-point FFT. (d) 1024-point FFT. Gray contour scale is normalized gain magnitude.

is not centered in the FFT bins. Spreading between frequency bins will occur which raises the noise floor, thus making it difficult to discern signals in neighboring frequencies and therefore degrades dynamic range.

A fixed-point MATLAB FPGA model was written to model the digital beamforming system from the input of the ADC to the output of the beamforming computation. The model was used to determine the effects of bit truncation on dynamic range and sensitivity. The simulation was first tested with high precision bits to determine how the dynamic range and sensitivity performance compared with theory. Those results are shown in the text of Fig. 6. The FPGA platform being used (see Fig. 5) has limited I/O lines at the output of the intermediate FPGA chips (66 b out of the calibration block) and the output of the final FPGA chip (108 b out of the matrix multiply and power calculation) creating a need to truncate in order to implement the design in hardware. Simulations were performed to determine the impact of the truncation at both points in the algorithm. For this system, it was necessary to truncate the output of the calibration block to 8 b and the output of the matrix multiply to 16 b. Dynamic range performance shown in Fig. 6 was dominated by the truncation after the calibration and is the limiting factor in system performance.

V. System Performance and Discussion

In this section, several results are presented for the smart antenna receiver system, including calibration, FPGA implementation, and system trades. The FPGA architecture shown in Fig. 5 is verified through an end-to-end VHDL simulation along with actual hardware implementation to determine the chip resources and speed. The FPGA procedure for computing the calibration weights (see Fig. 4) was not implemented in this paper but is planned to be added to the current FPGA architecture. Since the calibration procedure utilizes the same FFT as in Fig. 5, the rest of the arithmetic should easily fit into the current FPGAs.

For calibration (see Fig. 2), an experiment was performed to show the validity of using one calibration frequency to calibrate over a wide range of frequencies. For this experiment, several tones with frequencies ranging from 1.8 to 2 GHz were received at broadside and calibrated with respect to the 1.92-GHz calibration signal. Fig. 7 shows the processed measured results from 1.8 to 2 GHz in increments of 10 MHz. The processed antenna pattern is well behaved at all frequencies even though it was calibrated with respect to only one frequency. This 200-MHz frequency range represents a 10% bandwidth for this system. For systems with greater than 10% bandwidths, using a single calibration frequency may not be valid.

The FPGA approach presented in this paper (see Fig. 5) is capable of employing 16-, 64-, 256-, or 1024-point FFT FPGA cores. Since the 1024-point FFT requires more FPGA resources than the smaller FFTs, it was implemented first to determine how many FPGAs are required in the system. Fig. 8 shows the frequency resolution versus FFT size calculated for several bandpass sampling scenarios. For this experiment, the sampling rate was $f_S = 80.842$ MHz with an ideal bandwidth of 40 MHz (actual bandwidth was 25 MHz when excluding the 7.5-MHz guard bands). To demonstrate the effects of FFT size on frequency resolution, a 10-MHz linear FM waveform was transmitted through the system and processed for all four FFT cases. Fig. 9 shows a single channel of the processed linear FM waveform. It is clear from both Figs. 8 and 9 that the 1024-point FFT has more than adequate frequency resolution for this system and significantly better performance than the 16-, 64-, and 256-point FFTs.

An FPGA VHDL simulation for Fig. 5 compared with a full precision MATLAB FPGA model is shown in Fig. 10. Here the system input was a two-tone signal at 1.92 GHz, with 0° and -43° angles of arrival. The two-tone signal was generated in MATLAB, including the actual RF amplitude and phase errors, and quantized with an 8-b ADC at 80.842 MHz. For the FPGA implementation, there are a total of 25 scan angles from -60° to $+60^\circ$ in 5° steps. With a 13° half power beamwidth, 5° beam steering resolution is adequate for system operation.

The main application of the smart antenna receiver system presented in this paper is to employ digital beamforming for direction finding of signals arriving over a wide range of angles at various frequencies. Fig. 11 shows a simulated scenario using the MATLAB FPGA model for five received signals utilizing 16-, 64-, 256-, and 1024-point FFTs. The five users were generated at the following frequencies and angles of arrival:

1) 1.92 GHz at 0°;
2) 1.9205 GHz at -5°;
3) 1.921 GHz at -10°;
4) 1.919 GHz at 5°;
5) 1.918 GHz at 10°.

With the 1024-point FFT case, all five signals are resolved. For the other cases, 16-, 64-, and 256-point FFTs, only two, three, and four signals are resolved, respectively.

VI. Conclusion

This paper has shown that a smart antenna system with digital beamforming and FPGA processing is possible today with a moderate number of channels and angles. The feasibility of an eight-channel system was proven in hardware. Two calibration methods were compared and both were demonstrated with measured data captured by the smart antenna receiver system.

This system uses the Virtex-E. Today much larger FPGA parts are available. For a state-of-the-art FPGA, such as the Xilinx Virtex-II (XC2V10000) [16], there exists 1108 I/Os and real estate for 25+ 1024-point FFTs. This would allow a digital beamforming system with eight antenna elements to be implemented in real time with two devices. With advances in FPGAs and ADCs, it will soon be practical and cost-effective to build larger smart antenna systems with reconfigurable applications.

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